REMARKS

Claims 14-25, and 29-59 are pending.

Claims 14-25 and 29-59 stand rejected.

Claims 14, 16-18, 20-22, 29, 33, 36, 40, 46, and 52-54 are amended. No new subject matter is added. It is believed that the amendments place the claims in condition for allowance. The Examiner is thanked for the time spent discussing this application by phone interview on March 20, 2003. If the amendments fail to place the application in condition for allowance it is respectfully requested that the Examiner contact Todd Iverson at the phone number given at the end of this response.

Reconsideration and allowance of the pending claims is respectfully requested in light of the following remarks.

Claim Rejections – 35 USC § 103

Claims 14, 16-18, 20-22, 24-25, 29-37, 40-41, 43-44, 46-47, 49-50, 54-56, 58-59 are rejected under 35 U.S.C. 103(a) as being unpatentable over Admitted Prior Art (APA) in view of Nagamine (5,534,724) and Bothra et al. (6,020,616).

Amended claim 14 recites, in part, a plurality of active regions each having at least two transistors and a plurality of dummy gates located between the at least two transistors.

The APA does not disclose a plurality of dummy gates (FIG. 5).

Nagamine does not disclose a plurality of dummy gates located between the at least two transistors (FIGS. 3 and 4).

Bothra discloses a plurality of dummy polysilicon lines 226 but they are located on the outside of the active regions 204 and are substantially isolated from the active regions 204 (Fig. 3L, column 8, lines 8-11). Thus, Bothra does not disclose a plurality of dummy gates located between the at least two transistors on each active region.

Consequently, the combination of APA, Nagamine, and Bothra fails to disclose each element of claim 14 and a *prima facie* case of obviousness is not established. Claims 16 and 17 are amended to be consistent with claim 14. Claims 15-17 are believed to be allowable for at least the same reason as claim 14.

Amended claim 18 recites, in part, a plurality of active regions each having at least two transistors and a plurality of dummy gates located between and to either side of the at least two transistors.

The APA does not disclose a plurality of dummy gates (FIG. 5).

Nagamine does not disclose a plurality of dummy gates located between and to either side of the at least two transistors (FIGS. 3 and 4).

Bothra discloses a plurality of dummy polysilicon lines 226 but they are located only on the outside of the active regions 204 and are substantially isolated from the active regions 204 (Fig. 3L; column 8, lines 3-11). Thus, Bothra does not disclose a plurality of dummy gates located between and to either side of the at least two transistors in the active regions.

Consequently, the combination of APA, Nagamine, and Bothra fails to disclose each element of claim 18 and a *prima facie* case of obviousness is not established. Claims 20 and 21 are amended to be consistent with claim 18. Claims 19-21 are believed to be allowable for at least the same reason as claim 18.

Amended claim 22 recites, in part, a plurality of active regions comprising at least two transistors, a plurality of dummy gates located not between but to both sides of the at least two transistors, at least two dummy gates separated from an adjacent transistor gate by a substantially identical gap, and each of the dummy gates separated from another dummy gate by the same substantially identical gap.

The APA does not disclose a plurality of dummy gates (FIG. 5).

Nagamine does not disclose a plurality of dummy gates located not between but to both sides of the at least two transistors (FIGS. 3 and 4).

Bothra discloses a plurality of dummy polysilicon lines 226 located to both sides of active regions 204. However, Bothra does not disclose that there are at least two dummy polysilicon lines 226 separated from an adjacent polysilicon line 216 by a substantially identical gap (FIG. 3L; column 8, lines 3-11).

Consequently, the combination of APA, Nagamine, and Bothra fails to disclose each element of claim 22 and a *prima facie* case of obviousness is not established. Claims 23-28 are believed to be allowable for at least the same reason as claim 22.

Amended claim 29 recites, in part, a plurality of active regions on a substrate, a portion on the substrate other than the active region, a plurality of transistor gates formed on the active regions with a first gap between adjacent transistor gates, a plurality of dummy gates formed on the portion other than the active region that are characterized as having a second gap between adjacent dummy gates and a third gap between at least two dummy gates and a corresponding adjacent transistor gate, and wherein the first, second, and third gaps are substantially identical.

The APA does not disclose a plurality of dummy gates but does disclose a first gap between adjacent transistor gates (FIG. 5).

Nagamine discloses a plurality of dummy wiring lines 20 and a second gap between adjacent dummy wiring lines. However, Nagamine does not disclose a third gap between at least two dummy gates and a corresponding adjacent transistor gate wherein the first, second, and third gaps are substantially identical (FIGS. 3 and 4).

Bothra discloses a plurality of dummy polysilicon lines 226 and a second gap between adjacent dummy polysilicon lines 226, but it does not disclose a third gap between at least two dummy polysilicon lines 226 and a corresponding adjacent transistor gate wherein the first, second, and third gaps are substantially identical. (FIG. 3L).

Consequently, the combination of APA, Nagamine, and Bothra fails to disclose each element of claim 29 and a *prima facie* case of obviousness is not established. Claims 30-32 are believed to be allowable for at least the same reason as claim 29.

Amended claim 33 recites, in part, a first transistor gate and a second transistor gate at the edge of a first active region and a second active region, respectively, separated from a respective first dummy gate and second dummy gate by a third and fourth gap, wherein the third and fourth gaps are substantially identical. It is apparent that neither APA (FIG. 5), Nagamine (FIG. 3), nor Bothra (FIG. 3L) disclose the recited limitation.

Consequently, the combination of APA, Nagamine, and Bothra fails to disclose each element of claim 33 and a *prima facie* case of obviousness is not established. Claims 34-36 are believed to be allowable for at least the same reason as claim 33.

Amended claim 36 recites, in part, a plurality of dummy gates disposed on the substrate between the at least two electrodes of the active regions.

APA does not disclose a plurality of dummy gates disposed on the substrate (FIG. 5).

Nagamine does not disclose a plurality of dummy gates disposed on the substrate between the at least two electrodes of the active regions. Conversely, the dummy wiring region 7 is shown located above, and not between, the gate electrodes 9b (FIG. 3).

Bothra does not disclose a plurality of dummy gates disposed on the substrate between the at least two electrodes of the active regions. Conversely, the dummy polysilicon lines 226 are located outside the active regions 204 (FIG. 3L).

Consequently, the combination of APA, Nagamine, and Bothra fails to disclose each element of claim 36 and a *prima facie* case of obviousness is not established. Claims 37-39 are believed to be allowable for at least the same reason as claim 36.

Amended claim 40 recites, in part, a plurality of transistor gates of a first width, a plurality of dummy gates of a second width, and a plurality of dummy gates of a third width, wherein each of the transistor gates is aligned along the same longitudinal axis as a

corresponding one of the dummy gates of the third width, and wherein the second width is greater than the sum of the first and the third widths. Support for this amendment is found in FIG. 12 of the application.

APA does not disclose a plurality of dummy gates of a second width and a plurality of dummy gates of a third width (FIG. 5), neither does Nagamine (FIG. 3). Bothra does not disclose a plurality of dummy gates of a second width, a plurality of dummy gates of a third width, nor that each of the transistor gates is aligned along the same longitudinal axis as a corresponding one of the dummy gates of the third width (FIG. 3L).

Consequently, the combination of APA, Nagamine, and Bothra fails to disclose each element of claim 40 and a *prima facie* case of obviousness is not established. Claims 41-45 are believed to be allowable for at least the same reason as claim 40.

Amended claim 46 recites, in part, a plurality of active regions having at least two transistors and at least two electrodes, a plurality of transistor gates disposed on the substrate between the at least two electrodes of the active regions, and a plurality of dummy gates with a first portion in contact with a bias line and at least one second portion extending in a vertical direction and arranged such that the at least one second portion is interspaced between adjacent transistor gates.

APA does not disclose a plurality of dummy gates (FIG. 5). Nagamine does not disclose a plurality of dummy gates with a first portion in contact with a bias line and at least one second portion extending in a vertical direction and arranged such that the at least one second portion is interspaced between adjacent transistor gates (FIG. 3). Bothra does not disclose that at least one second portion of the dummy gates are interspaced between adjacent transistor gates of the active regions (FIG. 3L).

Consequently, the combination of APA, Nagamine, and Bothra fails to disclose each element of claim 46 and a *prima facie* case of obviousness is not established. Claims 47-51 are believed to be allowable for at least the same reason as claim 46.

Amended claim 54 recites, in part, first dummy gates on said isolation portion aligned with said first transistor gates such that a portion of a first dummy gate extending in a first direction and a portion of a corresponding first transistor gate extending in the first direction share a common central axis. Neither APA (FIG. 5), Nagamine (FIG. 3), nor Bothra (FIG. 3L) disclose this limitation.

Consequently, the APA/Nagamine/Bothra combination fails to disclose each element of claim 54 and a *prima facie* case of obviousness is not established. Claims 55-59 are believed to be allowable for at least the same reason as claim 54.

Claims 15, 19, 23, 42, 45, 48, 51-53, and 57 stand rejected under 35 U.S.C. 103(a) as being unpatentable over APA, Nagamine, and Bothra et al., as applied to claims 14, 18, and 22 above, and further in view of Hansch et al. (6,174,741).

Claims 15, 19, 23, 42, 45, 48, and 51 were previously addressed with respect to the APA/Nagamine/Bothra combination. It is believed that these claims are allowable for at least the previously presented reasons.

Amended claim 52 recites, in part, a plurality of transistor gates and a plurality of dummy gates disposed on the substrate between at least two electrodes on an active region, where both the transistor gates and the dummy gates have a portion extending in a first direction and a plurality of portions extending in a second direction perpendicular to the first direction. Support for this amendment is found in the application (see FIGS 11-12).

APA does not disclose a plurality of dummy gates (FIG. 5). Nagamine does not disclose a plurality of dummy gates each with a portion extending in a first direction and a plurality of portions extending in a second direction perpendicular to the first direction (FIG. 3). Bothra does not disclose a plurality of dummy gates disposed between at least two electrodes on an active region, nor does it disclose a plurality of dummy gates each with a portion extending in a first direction and a plurality of portions extending in a second direction perpendicular to the first direction (FIG. 3L). Hansch fails to disclose these relevant limitations of claim 52 as well (FIG. 4).

Consequently, the APA/Nagamine/Bothra/Hansch combination fails to disclose each element of claim 52 and a *prima facie* case of obviousness is not established.

Amended claim 53 recites, in part, a plurality of transistor gates and a plurality of dummy gates disposed on the substrate between at least two electrodes on an active region, where both the transistor gates and the dummy gates have a portion extending in a first direction and a plurality of portions extending in a second direction perpendicular to the first direction. Support for this amendment is found in the application (see FIGS 11-12).

APA does not disclose a plurality of dummy gates (FIG. 5). Nagamine does not disclose a plurality of dummy gates each with a portion extending in a first direction and a plurality of portions extending in a second direction perpendicular to the first direction (FIG. 3). Bothra does not disclose a plurality of dummy gates disposed between at least two electrodes on an active region, nor does it disclose a plurality of dummy gates each with a portion extending in a first direction and a plurality of portions extending in a second

direction perpendicular to the first direction (FIG. 3L). Hansch fails to disclose these relevant limitations of claim 53 as well (FIG. 4).

Consequently, the APA/Nagamine/Bothra/Hansch combination fails to disclose each element of claim 53 and a *prima facie* case of obviousness is not established.

Claim 57 is dependent upon claim 54 and thus is allowable for at least the reasons given previously for claim 54.

Claims 38-39 stand rejected under 35 U.S.C. 103(a) as being unpatentable over APA, Nagimine, and Bothra et al., as applied to claims 36 and 37 above, and further in view of Neugebauer (5,748,835). Claims 38 and 39 are believed to be allowable for at least the same reasons previously given for claim 36.

Conclusion

For the foregoing reasons, reconsideration and allowance of claims 14-25 and 29-59 of the application as amended is solicited. The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Respectfully submitted,

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